WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate;

at least one actually used MIS transistor disposed in an active region within the semiconductor substrate;

a plurality of MIS transistors used for evaluation which are disposed in active regions within the semiconductor substrate, include respective gate electrodes, respective source regions, and respective drain regions, and are used to typify characteristics of the actually used MIS transistor;

a gate common conductive portion electrically connected to the respective gate electrodes of the MIS transistors used for evaluation;

a source common conductive portion electrically connected to the respective source regions of the MIS transistors used for evaluation; and

a drain common conductive portion electrically connected to the respective drain regions of the MIS transistors used for evaluation.

2. The device of Claim 1, wherein the MIS transistors used for evaluation are disposed in the active regions which are adjacent to each other.

3. The device of Claim 2, wherein the respective gate electrodes of the MIS transistors used for evaluation are a single, commonized gate electrode.

4. The device of Claim 3, further comprising:

an interlayer dielectric film interposed in between where the source and drain common conductive portions are and where the source and drain regions of the MIS

transistors used for evaluation are; and

plugs passing though the interlayer dielectric film to establish connection between the source common conductive portion and the source regions and between the drain common conductive portion and the drain regions,

wherein the source and drain common conductive portions have branched head portions that are connected to the plugs.

5. The device of Claim 3 or 4, further comprising dummy electrodes which are formed to both sides of the gate electrode of the MIS transistors used for evaluation, are arranged substantially in parallel with the gate electrode, and do not function as gates.

6. The device of Claim 2, wherein the active regions, in which the MIS transistors used for evaluation are disposed, are arranged substantially in a row, and dummy active regions, in which no MIS transistors are present, are formed respectively alongside two of the active regions, the two regions being the endmost of the active regions.

7. The device of Claim 1, wherein the MIS transistors used for evaluation have substantially the same structure as that of the actually used MIS transistor.

8. The device of Claim 7, wherein the actually used MIS transistors are grouped into a plurality of types of actually used MIS transistors having substantially different structures; and

the MIS transistors used for evaluation are grouped into a plurality of types of MIS transistors used for evaluation that are substantially the same in structure as the plurality of types of actually used MIS transistors.

9. The device of Claim 1, wherein the active regions in which the MIS transistors used for evaluation are disposed have a larger dimension in the gate-length direction than that of the active region in which the actually used MIS transistor is disposed.

10. The device of Claim 6, wherein the active regions, in which the MIS transistors used for evaluation are disposed, and the dummy active regions have a larger dimension in the gate-length direction than that of the active region in which the actually used MIS transistor is disposed.

11. A method for evaluating characteristics of a semiconductor device which includes a semiconductor substrate and an actually used MIS transistor disposed in an active region within the semiconductor substrate, the method comprising the steps of:

(a) dividing a wafer into a plurality of blocks each including a plurality of MIS transistors used for evaluation, evaluating characteristics of the MIS transistors used for evaluation for each said block, and storing evaluation results in a memory; and

(b) calculating, for each said block, an average value of the characteristics of the MIS transistors used for evaluation from the evaluation results stored in the memory in the step (a), and storing calculation results in the memory.

12. The method of Claim 11, wherein

the wafer includes a gate common conductive portion electrically connected to respective gate electrodes of the MIS transistors used for evaluation, a source common conductive portion electrically connected to respective source regions of the MIS transistors used for evaluation, and a drain common conductive portion electrically

connected to respective drain regions of the MIS transistors used for evaluation, and

in the step (b), the average value of the characteristics of the MIS transistors used for evaluation that are connected to the gate common conductive portion, the source common conductive portion and the drain common conductive portion is calculated.

13. The method of Claim 11, wherein in the step (a), the MIS transistors used for evaluation are disposed in scribe areas of the wafer.